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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/585,576	08/23/2006	Kazuya Uejima	065686-0163	4297
22428	7590	11/13/2008	EXAMINER	
FOLEY AND LARDNER LLP			NGUYEN, DUY T V	
SUITE 500				
3000 K STREET NW			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20007			4136	
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			11/13/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/585,576	UEJIMA, KAZUYA	
	<b>Examiner</b>	<b>Art Unit</b>	
	DUY T. NGUYEN	4136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_\_.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_ is/are allowed.  
 6) Claim(s) 1-17 is/are rejected.  
 7) Claim(s) 2 is/are objected to.  
 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
     1. Certified copies of the priority documents have been received.  
     2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
     3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>8/23/2006 &amp; 7/10/2006</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
|  | 6) <input type="checkbox"/> Other: _____                          |

***DETAILED ACTION***

***Claims Objections***

1. Claim 2 is objected because of the following reasons:

In claim 2, lines 9 and 10, "a portion under gate side wall and gate electrode has a greater film thickness than any other portion" in which "a portion" and "any other portion" are unclearly claimed and described in the specification. Based on the prior arts, the examiner assumes that any portion under the gate side wall and the gate electrode including the thicknesses of substrate layer, cap layer, channel layer, buffer layer or oxide layer can be applied in making a rejection.

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4, 6-10, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable Sugiyama et al. (US Patent Pub. 2004/0070051, from hereinafter "Sugiyama") in view of Noda (US Patent Pub. 2002/0058385).

Regarding claims 1-4, and 14 Sugiyama teaches, as shown in Figs. 1, 3 and 5A-5E, claim 20 and paragraphs 0036-0039, 0054-0056, 0066, 0069-0080, and 0084, an MIS-type field-effect transistor characterized in comprising: a base layer (101, 102, 103); a strained

active semiconductor layer (104, 114) formed on said base layer (101, 102, 103); a gate insulating film (105, 116) formed on said active semiconductor layer (104, 114); a gate electrode (106, 117) formed on said gate insulating film (105, 116); and a source/drain region (107, 118) formed in portions on both sides of said gate electrode (106, 117) inside said active semiconductor layer (104, 114); a gate side wall formed on the lateral face of said gate electrode (106, 117) (see Fig. 3); wherein a portion under said gate side wall and said gate electrode of said active semiconductor layer has a greater film thickness than any other portion (see Figs. 5A-5E, paragraphs 0069-0080); and a built-up layer (151) provided with a source/drain (118) and formed on said active semiconductor layer (104, 114) on both sides of said gate electrode (106, 117). In addition, Suglyama also teaches the thickness of the channel layer (104, 114) (not smaller than 3 nm and 5nm, paragraphs 0055-0056), the source/drain (107, 118) (not more than 35 nm, paragraph 0066), and the built-up layer (151) thickness (up to about 100 nm, paragraph 0084).

However, Suglyama fails to specifically teach an interface between said base layer and said active semiconductor layer is at a depth of  $2Tp$  or less from the surface; a built up-layer has a film thickness of  $3Tp$  or greater (and/or  $5Tp$ ), where  $Tp$  is the depth of maximum concentration of an impurity introduced for forming said source/drain region; the source/drain region is formed by an ion implantation method.

Noda teaches the different doses of ion implantations, the process of forming source/drain; and the source/drain region is formed by an ion implantation method (see paragraphs 0059, 0066-0068, 0070, and 0092).

In view of the teaching of Noda, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Noda in Suglyama

structure in order to have an interface between said base layer and said active semiconductor layer is at a depth of 2Tp or less from the surface, the build-up layer has a film thickness of 3Tp (and /or 5Tp) or greater, where Tp is the depth of maximum concentration of an impurity introduced for forming said source/drain region; and the source/drain region is formed by an ion implantation method, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). In addition, it is favorable to have an object to realize miniaturization by suppressing the dose loss phenomenon after impurity ion implantation (see Noda, paragraph 0011).

Regarding to claims 6-8, as shown in Fig. 1, paragraph 0037, and Fig. 5A, paragraph 0069, Suglyama teaches the base layer is an Si layer; the base layer is a semiconductor layer, and an insulator layer is formed underneath said base layer; base layer is an insulator layer.

Regarding claims 9 and 10, Suglyama teaches the active semiconductor layer is a group IV semiconductor layer (Si, Ge and/or SiGe); and active semiconductor is an Si layer (see paragraphs 0037, 0139, claims 1 and 20).

Regarding claim 13, Suglyama teaches the gate length is not greater than 100nm (0.1 um) (see paragraph 0065).

"[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) (MPEP Chapter 2100-Section 2144.05-Optimization of Ranges).

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable Suglyama as modified by Noda and further in view of Guarini et al. (US Patent Pub. 2004/0241958, from hereinafter "Guarini"). The teachings of Suglyama/Noda have been discussed above.

Regarding claim 5, Suglyama/Noda fail to teach the base layer is a semiconductor layer having the composition  $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  (wherein  $0 \leq x \leq 1$ ,  $0 \leq y \leq 1$ , and  $0 < x + y \leq 1$ ).

Guarini teaches, as shown in Figs. 1 & 2, teaches the base layer is a semiconductor layer having the composition  $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  (see page 2, paragraphs 0027, 0028, and 0030).

In view of the teaching of Guarini, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the substrate as taught by Guarini in Suglyama/Noda to achieve the base layer having the composition  $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  (wherein  $0 \leq x \leq 1$ ,  $0 \leq y \leq 1$ , and  $0 < x + y \leq 1$ ), since it is well-known to those skilled in the art in achieving a low temperature in forming a semiconductor device.

4. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable Suglyama as modified by Noda and further in view of Kubo et al. (US Patent Pub. 2003/0102490, from hereinafter "Kubo"). The teachings of Suglyama/Noda have been discussed above.

Regarding claim 11, Suglyama/Noda fail to teach the active semiconductor layer is a semiconductor layer having the composition  $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  (wherein  $0 \leq x \leq 1$ ,  $0 \leq y \leq 1$ , and  $0 < x + y \leq 1$ ).

Kubo teaches  $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  (wherein  $0 \leq x \leq 1$ ,  $0 \leq y \leq 1$ , and  $0 < x + y \leq 1$ ) (see page 5, paragraph 0084).

In view of the teaching of Kubo, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the composition of the active semiconductor layer as taught by Kubo. It is appropriate to combine Suglyama/Noda/Kubo because they teach the structure that allow one having skill in the art would result in

providing a transistor having a good characteristics while ensuring a sufficient reliability (see paragraph 0008).

Regarding claim 12, Suglyama teaches an Si layer with a film thickness not more than 2nm, 20nm or about 5nm, (see paragraphs 0062, 0114, and 0136).

5. Claim 15 is rejected under under 35 U.S.C. 103(a) as being unpatentable Suglyama as modified by Noda and further in view of Tanaka et al. (US Patent Pub. 2003/0134459, from here in after "Tanaka"). The teachings of Suglyama/Noda have been discussed above.

Regarding claim 15, Suglyama/Noda fail to teach source/drain region is formed by a plasma doping method.

Tanaka teaches source/drain region is formed by a plasma doping method (see page 2, paragraph 0035).

In view of the teaching of Tanaka, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the plasma doping method in forming source/drain region. It is favorable to minimize adverse effects on such a device of an impurity contained in the crystalline silicon film (see paragraph 0002).

6. Claim 16 is rejected under under 35 U.S.C. 103(a) as being unpatentable Suglyama as modified by Noda and further in view of Wiener et al. (US Patent No. 6,303,446, from hereinafter "Wiener"). The teachings of Suglyama/Noda have been discussed above.

Regarding claim 16, Suglyama/Noda fail to teach the source/drain region is formed by a gas- phase doping method.

Wiener teaches the source/drain region is formed by a gas- phase doping method (see abstract and col. 2, lines 63-65).

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In view of the teaching of Wiener, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the gas phase doping method on forming the source/drain region. It is favorable to form the source/drain region in one step by eliminating the intermediate oxide deposition and etch steps.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable Suglyama as modified by Noda and further in view of Ishii et al. (US Patent No. 6,492,680, from hereinafter “Ishii”). The teachings of Suglyama/Noda have been discussed above.

Regarding claim 17, Suglyama/Noda fail to teach a portion of the source/drain region near the gate electrode is a region of low impurity concentration.

Ishii teaches a source side low concentration impurity region and a drain side lower impurity concentration region are provided at lower sides of both end portion of the gate electrode (see col. 6, lines 16-35).

In view of the teaching of Ishii, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the source/drain as taught by Ishii in Suglyama/Noda structure. It is favorable to have the variation in the drain current to gate bias becomes small and constant current output characteristics of the MOS transistor element can be stabilized (see col. 2, lines 59-62).

### ***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to application's disclosure: US Patent No. 7,141,477 to Noda which discloses MIS semiconductor devices capable of accomplishing a further miniaturization and operating with high speed and lower power consumption.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DUY T. NGUYEN whose telephone number is (571) 270-7431. The examiner can normally be reached on Monday-Friday, 7:30 Am - 5:00 Pm (alternative Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lisa M. Caputo can be reached on (571) 272-2388. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DUY T NGUYEN/  
Examiner, Art Unit 4136

/Lisa M. Caputo/  
Supervisory Patent Examiner, Art Unit 4136